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Lahiri

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(54) **CHARGE PUMP CIRCUIT FOR A PHASE LOCKED LOOP**

(71) Applicant: **STMicroelectronics International N.V.**, Amsterdamn (NL)

(72) Inventor: **Abhirup Lahiri**, Delhi (IN)

(73) Assignee: **STMicroelectronics International N.V.**, Amsterdam (NL)

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H03L 7/06 (2006.01)
H03L 7/085 (2006.01)

(52) **U.S. Cl.**
CPC ***H03L 7/085*** (2013.01)

(58) **Field of Classification Search**
USPC 327/147–149, 156–158
See application file for complete search history.

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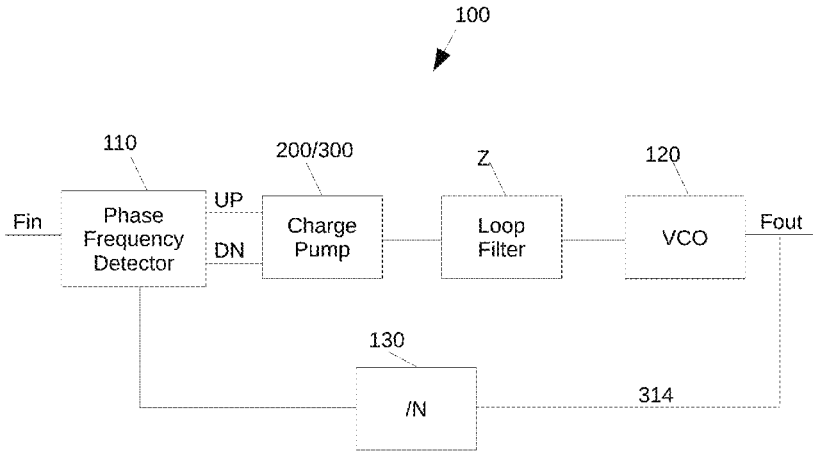
Primary Examiner — Adam Houston
(74) *Attorney, Agent, or Firm* — Gardere Wynne Sewell LLP

(57) **ABSTRACT**

A phase-locked-loop includes a phase-frequency-detector (PFD) comparing phases of an input signal and feedback signal, and generating therefrom control signals. An attenuation circuit in series with the PFD includes a filter between a voltage-controlled-oscillator (VCO) control node and ground. A buffer is coupled to the VCO control node. An impedance network is coupled to the VCO control node and has an impedance element coupled to a first current source so voltage at the VCO control node increases when control signals indicate the phase of the input signal leads the feedback signal, and coupled to a second current source so voltage at the VCO control node decreases when control signals indicate a lagging phase. A VCO is coupled to the VCO control node to generate an output signal, with the phase of the output signal matching the input signal. The feedback signal is based upon the output signal.

20 Claims, 7 Drawing Sheets



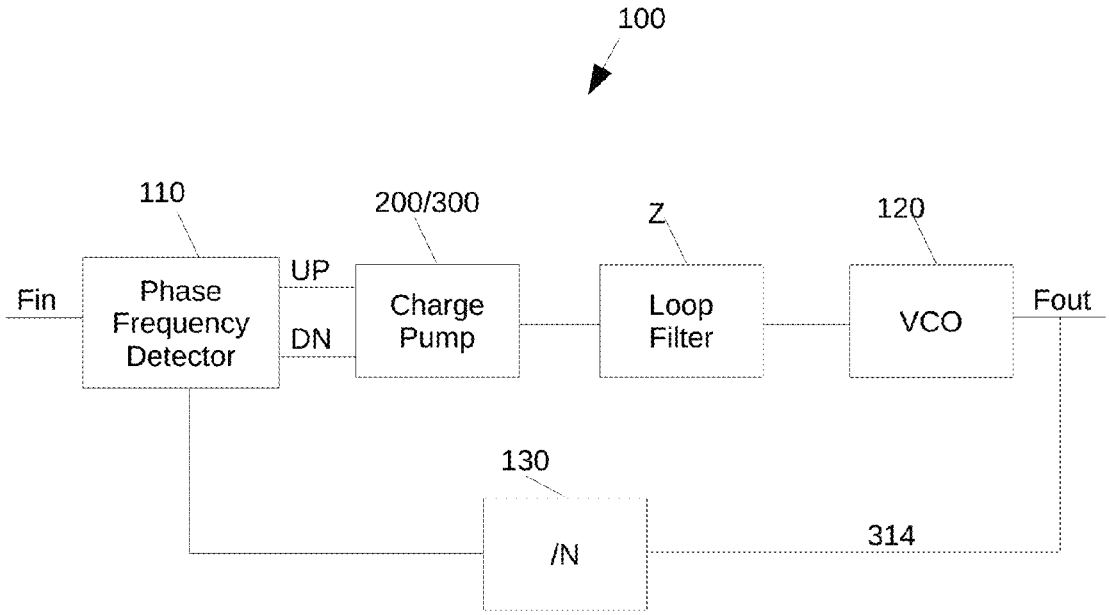

100
110
200/300
Z
120
Fin
Phase Frequency Detector
UP
DN
Charge Pump
Loop Filter
VCO
Fout
130
/N
314

FIG. 1

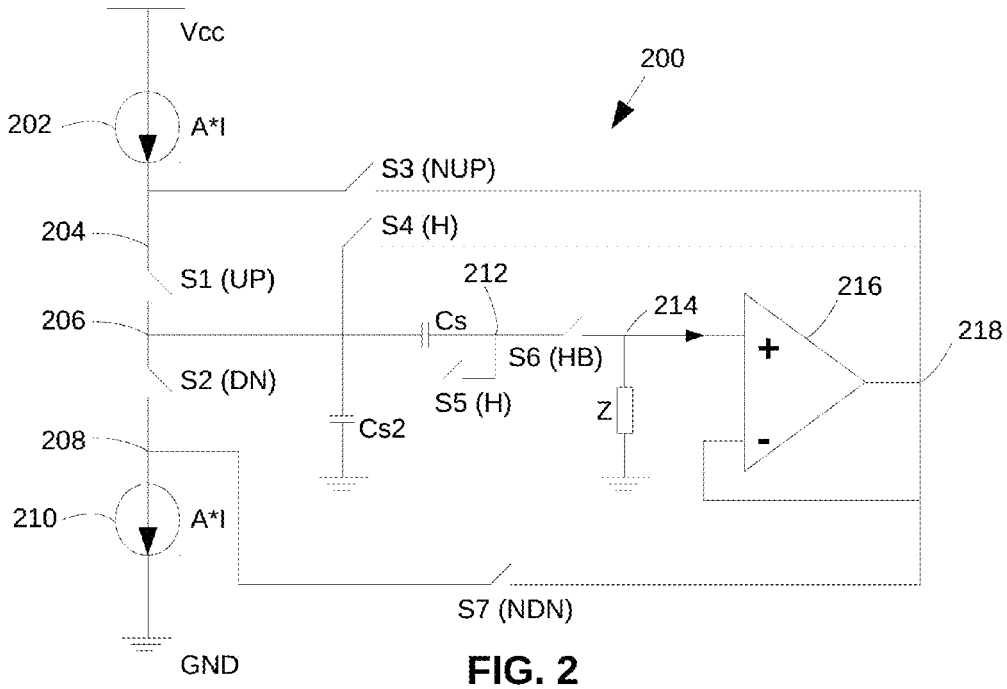


FIG. 2

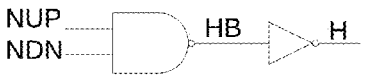


FIG. 2A

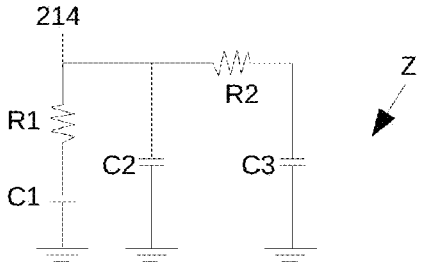


FIG. 3

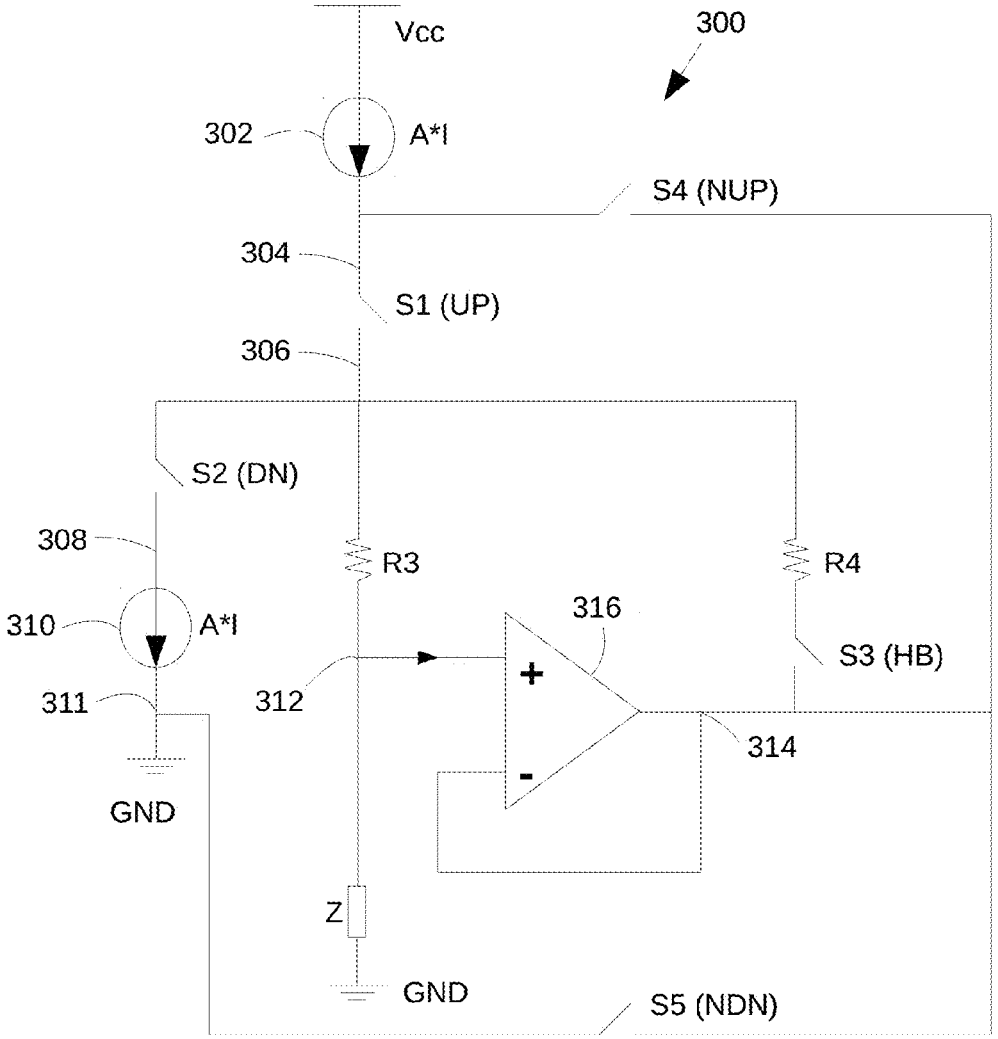

Vcc
300
302
A*I
S4 (NUP)
304
S1 (UP)
306
S2 (DN)
308
R3
R4
316
310
A*I
S3 (HB)
312
311
314
GND
Z
GND
S5 (NDN)

FIG. 4

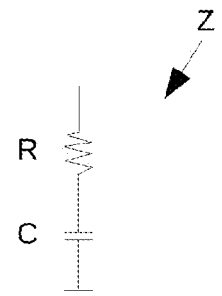

Z
R
C

FIG. 5

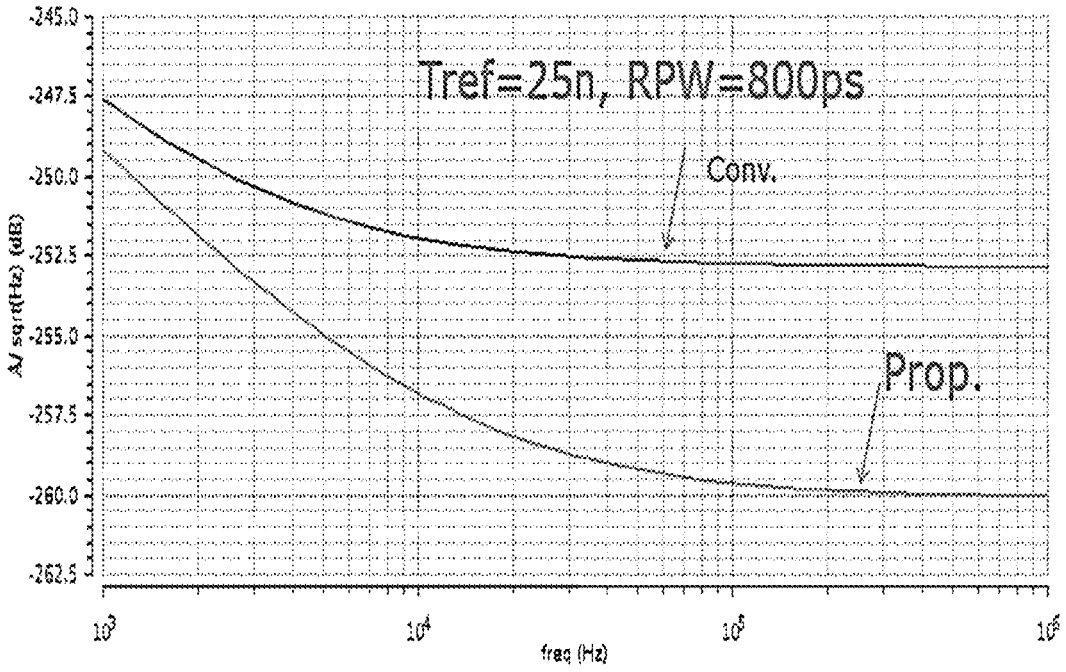

Tref=25n, RPW=800ps
Conv.
Prop.
-245.0
-247.5
-250.0
-252.5
-255.0
-257.5
-260.0
-262.5
Aj sqrt(Hz) (dB)
freq (Hz)

FIG. 6

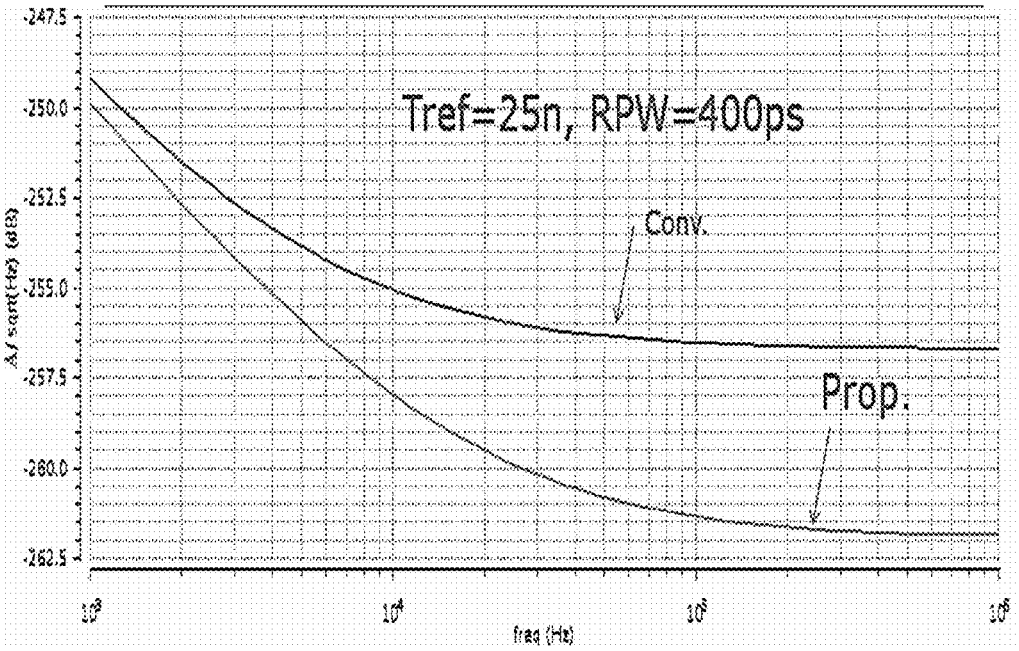

Tref=25n, RPW=400ps
Conv.
Prop.
-247.5
-250.0
-252.5
-255.0
-257.5
-260.0
-262.5
freq (Hz)

FIG. 7

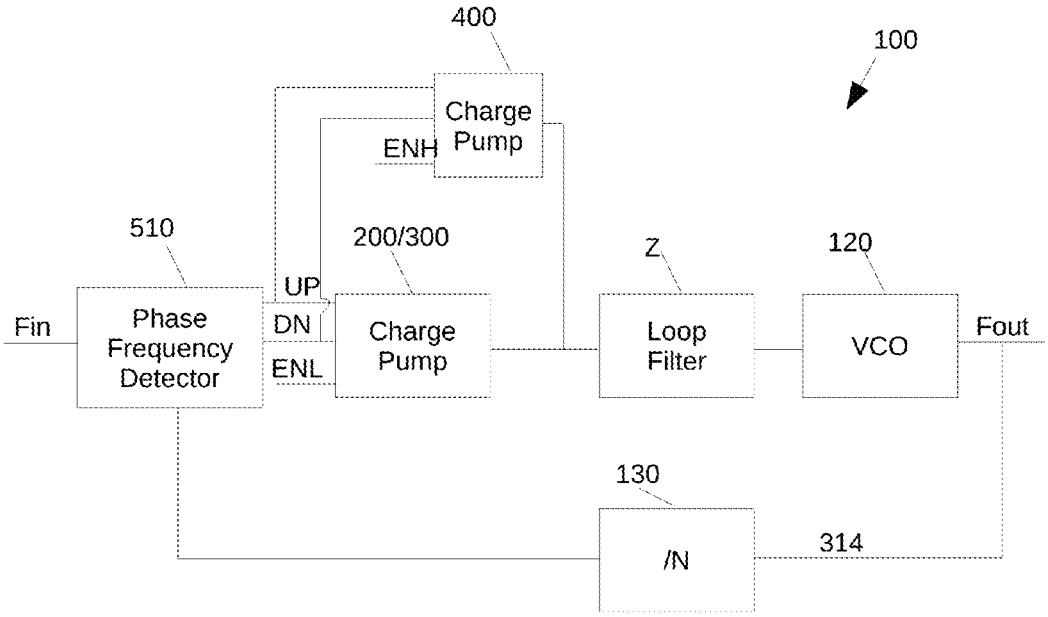

400
100
Charge Pump
ENH
510
200/300
Z
120
UP
Fin
Phase Frequency Detector
DN
ENL
Charge Pump
Loop Filter
VCO
Fout
130
/N
314

FIG. 8

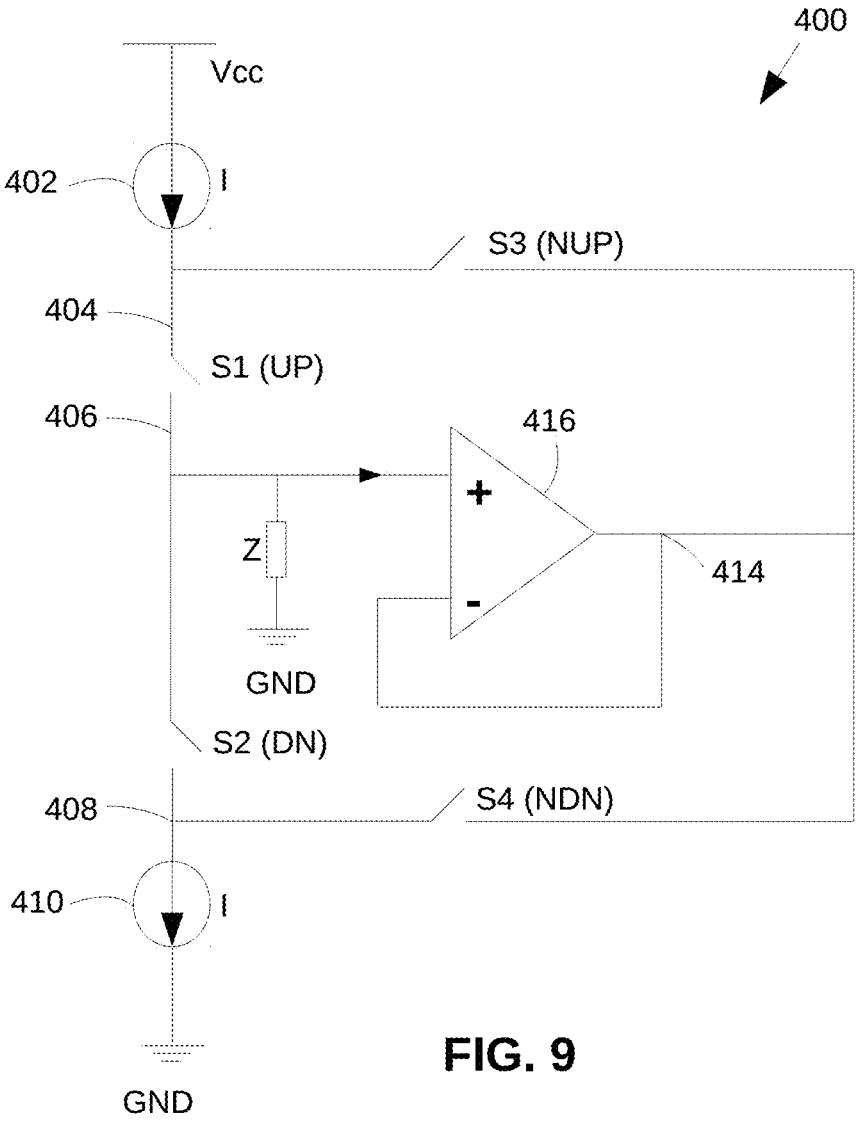

400
Vcc
402
I
S3 (NUP)
404
S1 (UP)
406
416
+
Z
-
414
GND
S2 (DN)
408
S4 (NDN)
410
I
GND

FIG. 9

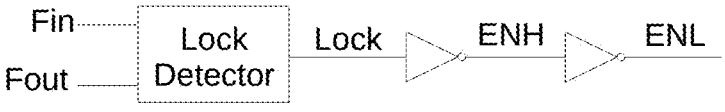

Fin
Fout
Lock Detector
Lock
ENH
ENL

FIG. 10

CHARGE PUMP CIRCUIT FOR A PHASE LOCKED LOOP

TECHNICAL FIELD

This disclosure is related to the field of phase locked loops, and, more particularly, to a charge pump circuit for phase locked loops.

BACKGROUND

A phase locked loop (PLL) is a control system that generates an output signal whose phase is related to the phase of an input signal. A typical phase locked loop includes a variable frequency oscillator and a phase detector. The oscillator generates a periodic signal. The phase detector compares the phase of the input signal with the phase of the periodic signal and generates control signals that adjust the oscillator to keep the phases matched.

Keeping the input and output phases locked also implies keeping the input and output frequencies the same. Consequently, in addition to synchronizing phases between signals, a phase locked loop can track an input frequency, or it can generate a frequency that is a multiple of the input frequency.

Such phase locked loops are widely employed in radio, telecommunications, computers and other electronic applications. They can be used to demodulate a signal, recover a signal from a noisy communication channel, generate a stable frequency at multiples of an input frequency (frequency synthesis), or distribute precisely timed clock pulses in digital logic circuits such as microprocessors. Since a single integrated circuit can provide a complete phase locked loop building block, phase locked loops are widely used in modern electronic devices, with output frequencies from a fraction of a hertz up to many gigahertz.

In some cases, it may be desirable for a phase locked loop to be operable over a wide band of frequencies. In order to produce such wide band phase locked loops, a charge pump circuit is typically employed in the loop to generate the control signals sent to the oscillator. However, such charge pump circuits may be noisy, resulting in an undesirable amount of in-band noise.

Therefore, new phase locked loop designs with new charge pump circuits are desirable.

SUMMARY

This summary is provided to introduce a selection of concepts that are further described below in the detailed description. This summary is not intended to identify key or essential features of the claimed subject matter, nor is it intended to be used as an aid in limiting the scope of the claimed subject matter.

A phase locked loop includes a phase frequency detector (PFD) configured to compare phases of an input signal and a feedback signal, and to generate therefrom control signals. An attenuation circuit is coupled in series with the PFD and includes first and second current sources, and a loop filter coupled between a voltage controlled oscillator (VCO) control node and a ground node. A buffer has an input coupled to the VCO control node. An impedance network is coupled to the VCO control node and includes at least one impedance element configured to be coupled to the first current source such that voltage at the VCO control node increases, based upon the control signals indicating that the phase of the input signal leads the phase of the feedback signal, and coupled to the second current source such that the voltage at the VCO control node decreases, based upon the control signals indicating that the phase of the feedback signal leads the phase of the input signal. A VCO is coupled to the VCO control node and to generate an output signal based upon a signal at the VCO control node, with the phase of the output signal matching the phase of the input signal. The feedback signal is based upon the output signal.

Another aspect is directed to a circuit including a first current source coupled between a power supply node and a first node, and a first switch coupled between the first node and a second node and controlled by a first control signal. A second switch is coupled between the second node and a third node and controlled by a second control signal. A second current source is coupled between the third node and a ground node. A third switch is coupled between the first node and an output node and controlled by a complement of the first control signal. A fourth switch is coupled between the second node and the output node and controlled by a third control signal. A fifth switch is coupled between the second node and a fourth node and controlled by the third control signal. A first capacitor coupled between the second node and the fourth node, and a second capacitor coupled between the second node and ground. A sixth switch is coupled between the fourth node and a fifth node and controlled by an inverse of the third control signal. A loop filter coupled between the fifth node and ground. An amplifier has a non-inverting terminal coupled to the fifth node, an inverting terminal coupled to the output node, and an output terminal coupled to the output node. A seventh switch coupled between the output node and the third node and controlled by an inverse of the second control signal.

A further aspect is directed to a circuit including a first current source coupled between a power supply node and a first node, and a first switch coupled between the first node and a second node and controlled by a first control signal. A second switch is coupled between the second node and a third node and is controlled by a second control signal. A second current source is coupled between the third node and a ground node. A first resistor is coupled between the second node and a fifth node. A second resistor is coupled between the second node and a fourth node. A third switch is coupled between the fourth node and a sixth node and controlled by a third control signal. A loop filter is coupled between the fifth node and ground. An amplifier has a non-inverting terminal coupled to the fifth node, an inverting terminal coupled to the sixth node, and an output terminal coupled to the sixth node.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a phase locked loop.

FIG. **2** is a schematic diagram of a charge pump circuit such as may be used in the phase locked loop of FIG. **1**.

FIG. **2**A is a block diagram of a circuit that may be used to generate the control signals H and HB for the charge pump circuit of FIG. **2**.

FIG. **3** is a schematic diagram of a loop filter such as may be used in the phase locked loops of FIGS. **1** and **4**.

FIG. **4** is a schematic diagram of another charge pump circuit such as may be used in the phase locked loop of FIG. **1**.

FIG. **5** is a schematic diagram of a loop filter such as may be used in the phase locked loop of FIG. **4**.

FIG. **6** is a graph showing output current noise for the charge pump circuits described herein vs. conventional charge pump circuits.

FIG. **7** is another graph showing output current noise for the charge pump circuits described herein vs. conventional charge pump circuits.

FIG. **8** is a schematic diagram of another phase locked loop such as may employ the charge pump circuits of FIGS. **2** and **4**.

FIG. **9** is a schematic diagram of another charge pump circuit such as may be used in the phase locked loop of FIG. **8**.

FIG. **10** is a block diagram of a logic circuit to generate the selection signal for the charge pump circuit of FIG. **9**.

DETAILED DESCRIPTION

One or more embodiments will be described below. These described embodiments are only examples of implementation techniques, as defined solely by the attached claims. Additionally, in an effort to provide a focused description, irrelevant features of an actual implementation may not be described in the specification.

With reference to FIG. **1**, a phase locked loop **100** is now described. The phase locked loop **100** includes a phase frequency detector **110**, which receives an input signal Fin having an input frequency, and an output signal Fout having an output frequency. The output signal Fout received by the phase frequency detector **100** is the output signal Fout of the phase locked loop **100**. The phase frequency detector **100** has outputs UP, DN coupled to a charge pump **200** or **300**, also referred to as an attenuation circuit. The charge pump **200** or **300** in turn has an output coupled to a loop filter Z, which is in turn coupled to a voltage controlled oscillator (VCO) **120**. The output of the VCO **120** is coupled to the input of the phase frequency detector **110** via an optional divider **130**.

In operation, the phase frequency detector **110** compares the input signal Fin to the output signal Fout, and generates the control signals UP, DN for the charge pump **200** or **300** based thereupon. When the phase of the input signal Fin leads the phase of the output signal Fout, the control signal UP is asserted at a logic high, while the control signal DN remains at a logic low. Conversely, then when the phase is the input signal Fin lags the phase of the output signal Fout, the control signal DN is asserted at a logic high, while the control signal UP remains at a logic low. When the phase of the input signal Fin and the phase of the output signal Fout match, neither UP nor DN are asserted.

The charge pump **200** or **300** generates a control signal for the VCO **120**, which is passed through the loop filter Z, which extracts the low frequency content of the control signal. The VCO **120**, based on the control signal, adjusts the phase and frequency of the output signal Fout. When UP is asserted, the charge pump **200** or **300** increases the voltage of the control signal, as opposed to decreasing the voltage of the control signal when DN is asserted. Those of skill in the art will appreciate that since the phase of the input signal Fin cannot both lead and lag the phase of the output signal Fout, the phase frequency detector **110** will not simultaneously assert both UP and DN.

An optional divider **130** may be included in the feedback loop coupling the output signal Fout to the phase frequency detector **110**. The divider **130** serves to divide the frequency of the output signal Fout, thereby causing the frequency of the output signal Fout to be generated by the VCO **120** as a multiple of the frequency of the input signal Fin. For example, if the divider **130** divides the frequency by 2, in order for the phase frequency detector **110** to see that the input signal Fin and the feedback signal (the output signal Fout after being fed through the divider **130**) have a same frequency, the output signal Fout would have a frequency twice that of the input signal Fin. If the divider **130** is not present, or if the divider divides by 1, then the frequency of the output signal Fout will match the frequency of the input signal Fin.

Details of the charge pump **200** and loop filter Z will now be given with reference to FIG. **2**. The charge pump **200** includes a first current source **202** coupled between a power supply node Vcc and a node **204**. Switch S**1** is coupled between node **204** and node **206**. Switch S**2** is coupled between node **206** and node **208**. A second current source **210** is coupled between node **208** and ground. Switch S**3** is coupled between node **204** and node **218**. Switch S**4** is coupled between node **206** and node **218**. Switch S**7** is coupled between node **218** and node **210**.

A first capacitor Cs is coupled between node **206** and node **212**, and switch S**5** is coupled in parallel with the first capacitor Cs between node **206** and node **212**. A second capacitor Cs**2** is coupled between node **206** and ground GND. Switch S**6** is coupled between nodes **212** and **214**, and the loop filter Z is coupled between node **214** and ground. In addition, the non-inverting terminal of an amplifier **216** is coupled to node **214**, while the inverting terminal and output terminal of the amplifier **216** is coupled to the node **218**. The capacitors Cs and Cs**2** have a capacitance value less than a capacitance value of impedance elements used in the loop filter Z. The value of Cs**2** differs from that of Cs by a factor of one less than a desired gain A of the charge pump circuit **100**. That is, the value of Cs**2** is Cs*(A−1).

In operation, switch S**1** is triggered in response to assertion of UP, while switch S**2** is triggered in response to assertion of DN. Switch S**3** is triggered in response to assertion of a complement of UP, noted as NUP, while switch S**7** is triggered in response to assertion of a complement of DN, noted as NDN. Switch S**6** is triggered in response to assertion of a signal representing a logical NAND operation between the complement of UP and the complement of DN HB (shown in FIG. **2**A), while switches S**4** and S**5** are triggered in response to assertion of a signal H which is a complement of that signal.

Thus, when the phase of the input signal Fin leads the phase of the output signal Fout, the phase frequency detector **110** asserts UP while keeping DN low. The switches S**1**, S**6**, and S**7** are closed and the other switches opened, resulting in the flow of current from the first current source **202** through nodes **204** and **206** into the second capacitor Cs. This serves to charge up the second capacitor Cs with a voltage seen at node **214**. The buffer **216** has a unity gain, and thus passes the voltage seen at node **214** to its output at node **218**. The control signal for the VCO **120** is output from node **214**.

On the other hand, when the phase of the input signal Fin lags the phase of the output signal Fout, the phase frequency detector **110** asserts DN while keeping UP low. The switches S**2**, S**3**, and S**6** are thus closed and the other switches opened, resulting in the sinking of current from node **206**, and thus the discharge of the voltage at the second capacitor Cs. Therefore, the voltage at node **214** falls, which the buffer **216** passes to its output at node **218**. The control signal for the VCO **120** is output from node **214**.

Where the phase of the input signal Fin is matched to the phase of the output signal Fout, the phase frequency detector **110** asserts neither UP nor DN. Thus, switches S**3**, S**4**, S**5**, and S**7** close, while the other switches remain open. This serves to pass the current from the first current source **202**

through the node **204**, into node **218**, into node **208**, and to ground GND through the second current source **210**.

The charge pump circuit **200** described above provide a variety of advantages over traditional charge pump circuits. For example, the charge pump circuit **200** uses a charge-pump current **202** and **210** that is higher by a factor of A, but preserves the overall PLL loop gain by an attenuation factor of 1/A which is achieved via capacitive division. This is illustrated in FIGS. **6-7**. Shown in FIGS. **8**A-**8**C is how noise suppression increases as A increases. In addition, the thermal noise in the charge pump circuit **200** from the current sources **202** and **210** is reduced by a factor of A. Amplifier noise feedthrough to the loop filter Z is proportional to Cs*Vamp*Fin, where Fin is the input frequency to the PLL and where Vamp is the voltage at the non-inverting terminal of the amplifier **216**, and should be less than the noise from the current sources **202** and **210**. Thus, for the same loop gain in the charge pump circuit **200**, the noise entering the loop filter Z is reduced. This also serves to reduce the in-band phase noise. The reduction in output noise over conventional charge pump circuits is on the order of 1/A and can be seen in FIGS. **6-7**.

An alternate design for the charge pump circuit **300** is now described with reference to FIG. **3**. The charge pump circuit **300** includes a first current source **302** coupled between the power supply node Vcc and node **304**, and a switch S**1** coupled between the node **304** and a node **306**. A switch S**2** is coupled between the node **306** and a node **308**. A second current source **310** is coupled between the node **308** and ground GND. A resistor R**3** is coupled between the node **306** and a node **312**, and the loop filter Z is coupled between the node **312** and ground GND. A resistor R**4** is coupled between the node **306** and a node **314**, through switch S**3**. A buffer **316** has its non-inverting terminal coupled to node **312**, and its inverting terminal and its output coupled to the node **314**. The values of the resistor of the attenuation filter Z is high. A switch S**4** is coupled between node **304** and node **314**. Node **314** is coupled to node **311**.

The resistance of the resistor R**3** may equal (A−1)*R**4**, while the resistance of R**4** is chosen to reduce the noise contribution from the resistive attenuation network and make its noise contribution less than that of current sources **302** and **310**. To do so, R**4**>A/Gm, where Gm is the transconductance of the current sources **302** and **310**. This causes 1/A of the current from the current sources **302**, **310** to flow across R**3** and into the attenuation filter Z. The current sources **302**, **310** conduct A times more current than conventional charge pump current sources, thus the transconductance of the current sources **302**, **310** can be A times more than that of conventional charge pump current sources. In addition, when the resistors R**3** and R**4** have large values, the noise from the amplifier **316** that enters the attenuation filter Z is reduced.

In operation, switch S**1** is triggered in response to assertion of UP, while switch S**2** is triggered in response to assertion of DN. Switch S**3** is triggered in response to assertion of a logical NAND operation between complements of UP and DN, denoted as HB, while switch S**4** is triggered in response to a complement of assertion of UP and switch S**5** is triggered in response to a complement of assertion of DN.

Therefore, when the phase of the input signal Fin leads the phase of the output signal Fout, the phase frequency detector **110** asserts UP while keeping DN low. Switch S**1**, S**3**, and S**5** are then closed while switch S**2** and S**4** are open, resulting in the flow of current from the first current source **302** through node **306**, into the resistor R**3**, and into node **312**, thereby generating a voltage across the resistor R**3**, which is seen by the non-inverting terminal of the buffer **316** at node **312**, which passes the voltage at node **312** to its output at node **314**. The control signal for the VCO **120** is output from node **312**.

When the phase of the input signal Fin lags the phase of the output signal Fout, the phase frequency detector **110** asserts DN while keeping UP low. The switches S**2**, S**3**, and S**4** close while the switches S**1** and S**5** open, resulting in the sinking of current from node **306**. Therefore, the voltage at node **312**, and thus the voltage of the control signal for the VCO **120**, falls.

When the phase of the input signal Fin matches the phase of the output signal Fout, the phase frequency detector **110** asserts neither UP nor DN. Thus, switches S**4**, S**5** are closed, while switches S**1**, S**2**, S**3** remain open. This serves to couple output of the buffer **316** to the non-inverting terminal of the buffer **316** and to ground, lowering the voltage at node **312**, and thus the voltage of the control signal for the VCO **120**.

The loop filter Z of FIG. **5** is usable with the charge pump circuit **300**, and comprises a resistor R coupled in series with a capacitor C. When the loop filter Z is employed, the value of the resistor R**3** differs from that of the resistor R**4** by a factor of one less than a desired gain A of the charge pump circuit **300**. That is, the value of R**3** is R**4***(A−1).

The charge pump circuit **300** has the same advantages as the charge pump circuit **200** described above. As stated, the charge pump circuit **300** offers an increased gain over conventional charge pumps by a factor of A, yet reduces the loop gain within the charge pump circuit **300** by a factor of 1/A, so the overall loop gain for the phase locked loop **100** is preserved. In addition, the thermal current noise in the charge pump circuit **300** is increased by a factor of A or $\sqrt{A}$, but is attenuated by $1/A^2$ when entering the loop filter Z. The noise feed through from the amplifier **316** to the loop filter Z is proportional to $V_{amp}/A*R$. Thus, for the same loop gain in the charge pump circuit **300**, the noise entering the loop filter Z is reduced.

An embodiment where the phase locked loop **100** employs one of the charge pump circuits **200**, **300** described above as well as an additional charge pump circuit **400** is now described with reference to FIG. **8**. The phase locked loop **100** operates as the phase locked loop of FIG. **1**, however the additional charge pump circuit **400** is coupled in series between the PFD **110** and the loop filter Z before the phase locked loop **100** locks, while one of the charge pump circuits **200**, **300** is coupled in series between the PFD **110** and the loop filter Z after the phase locked loop **100** locks. The purpose of this selection between charge pump circuits **200**, **300** or **400** is so as to assist quick locking of the phase locked loop **100** while still receiving the advantages of the charge pump circuits **200**, **300** as described above. It should be noted that if the current output by the charge pump **400** is I, then the current output by the charge pump circuits **200**, **300** would be I*A. Selection of the charge pump circuit **200**, **300** or **400** is based upon a selection signal.

As shown in FIG. **10**, a selection signal LOCK is generated based on a lock detector detecting whether or not the phase locked loop **100** has locked, by comparing the input frequency Fin to the feedback signal. An inverse of this selection signal ENH is used to enable the charge pump circuit **400**, while an inverse of that signal ENL is used to enable the charge pump circuits **200**, **300**.

The charge pump circuit **400**, as shown in FIG. **9**, includes a first current source **402** coupled between a power supply node and node **404**. A first switch S**1** is coupled between node **404** and node **406**. An amplifier **416** has a non-

inverting terminal coupled to node **406**. A loop filter Z is coupled between node **406** and ground. The inverting terminal of the amplifier **416** is coupled to its output at node **414** so as to bias the amplifier **416** in a unity gain mode.

A switch S2 is coupled between node **406** and node **408**. A second current source **410** is coupled between node **408** and ground. A switch S3 is coupled between node **404** and node **414**, while a switch S4 is coupled between node **414** and node **408**. In operation, switch S1 is actuated by assertion of UP, while switch S2 is actuated by assertion of DN. Switch S3 is actuated by an inverse of UP, NUP, while switch S4 is actuated by an inverse of DN, NDN.

When the phase of the input signal Fin leads the phase of the output signal Fout, the phase frequency detector **110** asserts UP while keeping DN low. The switches S1, S4 are closed and the other switches opened, resulting in the flow of current from the first current source **402** through nodes **404** and **406** into the loop filter Z and the non-inverting terminal of the amplifier **416**, thereby increasing the voltage seen at the non-inverting terminal. Due to the unity gain of the amplifier **416**. The voltage seen at node **406** is passed to its output at node **414**. The control signal for the VCO **120** is at node **406**.

When the phase of the input signal Fin lags the phase of the output signal Fout, the phase frequency detector **110** asserts DN while keeping UP low. The switches S2, S3 are thus closed and the other switches opened, resulting in the sinking of current from node **406**. Therefore, the voltage at node **406** falls, which the buffer **416** passes to its output at node **414**. The control signal for the VCO **120** is at node **406**.

Where the phase of the input signal Fin is matched to the phase of the output signal Fout, the phase frequency detector **110** asserts neither UP nor DN. Thus, switches S3, S4 while the other switches remain open. This serves to pass the current from the first current source **402** through the node **404**, into node **414**, into node **408**, and to ground GND through the second current source **410**.

It should be understood that any of the loop filters Z described herein may be used with any of the embodiments described herein, and that other types of loop filters (i.e. active loop filters utilizing operational amplifiers) are also usable with any of the embodiments described herein.

While the disclosure has been described with respect to a limited number of embodiments, those skilled in the art, having benefit of this disclosure, will appreciate that other embodiments can be envisioned that do not depart from the scope of the disclosure as disclosed herein. Accordingly, the scope of the disclosure shall be limited only by the attached claims.

The invention claimed is:

1. A phase locked loop, comprising:

a phase frequency detector (PFD) configured to compare phases of an input signal and a feedback signal, and to generate therefrom control signals;

an attenuation circuit coupled in series with the PFD and comprising:

first and second current sources;

a loop filter coupled between a voltage controlled oscillator (VCO) control node and a ground node;

a buffer having an input coupled to the VCO control node;

an impedance network coupled to the VCO control node and comprising at least one impedance element configured to be:

coupled to the first current source such that voltage at the VCO control node increases, based upon the control signals indicating that the phase of the input signal leads the phase of the feedback signal, and

coupled to the second current source such that the voltage at the VCO control node decreases, based upon the control signals indicating that the phase of the feedback signal leads the phase of the input signal;

a VCO coupled to the VCO control node and to generate an output signal based upon a signal at the VCO control node, the phase of the output signal matching the phase of the input signal;

wherein the feedback signal is based upon the output signal.

2. The phase locked loop of claim **1**, wherein the control signals comprise first and second control signals; wherein the first control signal is asserted based upon the phase of the input signal leading the phase of the feedback signal; wherein the second control signal is asserted based upon the phase of the feedback signal leading the phase of the input signal; and wherein the impedance network further comprises:

a first impedance network switch coupled between a first impedance network node and the VCO control node, the first impedance network switch being actuated based upon a third control signal;

a second impedance network switch coupled between the first impedance network node and a second impedance network node, the second impedance network switch being actuated based upon a complement of the third control signal; and

a third impedance network switch coupled between the second impedance network node and an output of the buffer, the third impedance network switch being actuated based upon the complement of the third control signal;

wherein the at least one impedance element comprises a first capacitor coupled between the second impedance network node and ground, and a second capacitor coupled between the first impedance network node and a second impedance network node.

3. The phase locked loop of claim **2**, wherein the third control signal represents a result of a logical NAND operation between a complement of the first control signal and a complement of the second control signal.

4. The phase locked loop of claim **2**, wherein the first current source is coupled between a power supply node and a first attenuation circuit node; wherein the second current source is coupled between ground and a third attenuation circuit node; wherein the impedance network further comprises:

a first attenuation circuit switch coupled between the first attenuation circuit node and the output of the buffer, the first attenuation circuit switch being actuated based upon a complement of the first control signal,

a second attenuation circuit switch coupled between the first attenuation circuit node and a second attenuation circuit node, the second attenuation circuit switch being actuated based upon the first control signal,

a third attenuation circuit switch coupled between the second attenuation circuit node and the third attenuation circuit node, the third attenuation circuit switch being actuated based upon the second control signal,

a fourth attenuation circuit switch coupled between the output of the buffer and the third attenuation circuit node, the fourth attenuation circuit switch being actuated based upon an inverse of the second control signal.

5. The phase locked loop of claim 1, wherein the control signals comprise first and second control signals; wherein the first control signal is asserted based upon the phase of the input signal leading the phase of the feedback signal; wherein the second control signal is asserted based upon the phase of the feedback signal leading the phase of the input signal; wherein the first current source is coupled between a power supply node and a first attenuation circuit node; wherein the second current source is coupled between ground and a third attenuation circuit node; and wherein the impedance network further comprises:

a first attenuation circuit switch coupled between the first attenuation circuit node and a second attenuation circuit node, the first attenuation circuit switch being actuated based upon the first control signal;

a second attenuation circuit switch coupled between the second attenuation circuit node and the third attenuation circuit node, the second attenuation circuit switch being actuated based upon the second control signal;

a third attenuation circuit switch coupled between a fourth attenuation circuit node and the output of the buffer, the third attenuation circuit being actuated based upon a complement of a third control signal; and

wherein the at least one impedance element comprises a first resistor coupled between the second attenuation circuit node and the VCO control node, and a second resistor coupled between the second attenuation circuit node and a fourth attenuation circuit node.

6. The phase locked loop of claim 5, wherein the third control signal represents a result of a logical NAND operation between a complement of the first control signal and a complement of the second control signal.

7. The phase locked loop of claim 5, wherein the lop filter comprises a loop filter resistor coupled to the VCO control node, and a loop filter capacitor coupled between the loop filter resistor and ground.

8. The phase locked loop of claim 1, wherein the loop filter comprises:

a first loop filter resistor coupled to the VCO control node;

a first loop filter capacitor coupled between the first loop filter resistor and ground; and

a second loop filter capacitor coupled between the VCO control node and ground.

9. The phase locked loop of claim 8, wherein the loop filter further comprises:

a second loop filter resistor coupled between the VCO control node and a loop filter node; and

a third loop filter capacitor coupled between the loop filter node and ground.

10. The phase locked loop of claim 8, wherein the at least one impedance element comprises a capacitor having a capacitance less than a capacitance of the second loop filter capacitor.

11. A circuit, comprising:

a first current source coupled between a power supply node and a first node;

a first switch coupled between the first node and a second node and controlled by a first control signal;

a second switch coupled between the second node and a third node and controlled by a second control signal;

a second current source coupled between the third node and a ground node;

a third switch coupled between the first node and an output node and controlled by a complement of the first control signal;

a fourth switch coupled between the second node and the output node and controlled by a third control signal;

a fifth switch coupled between the second node and a fourth node and controlled by the third control signal;

a first capacitor coupled between the second node and the fourth node;

a second capacitor coupled between the second node and ground;

a sixth switch coupled between the fourth node and a fifth node and controlled by an inverse of the third control signal;

a loop filter coupled between the fifth node and ground;

an amplifier having a non-inverting terminal coupled to the fifth node, an inverting terminal coupled to the output node, and an output terminal coupled to the output node; and

a seventh switch coupled between the output node and the third node and controlled by an inverse of the second control signal.

12. The circuit of claim 11, wherein the third control signal represents a result of a logical NAND operation between a complement of the first control signal and a complement of the second control signal.

13. The circuit of claim 11, wherein the loop filter comprises:

a first loop filter resistor coupled to the fifth node;

a first loop filter capacitor coupled between the first loop filter resistor and ground; and

a second loop filter capacitor coupled between the fifth node and ground.

14. The circuit of claim 13, wherein the first and second capacitors each have a capacitance less than a capacitance of the second loop filter capacitor.

15. A circuit, comprising:

a first current source coupled between a power supply node and a first node;

a first switch coupled between the first node and a second node and controlled by a first control signal;

a second switch coupled between the second node and a third node and controlled by a second control signal;

a second current source coupled between the third node and a ground node;

a first resistor coupled between the second node and a fifth node;

a second resistor coupled between the second node and a fourth node;

a third switch coupled between the fourth node and a sixth node and controlled by a third control signal;

a loop filter coupled between the fifth node and ground; and

an amplifier having a non-inverting terminal coupled to the fifth node, an inverting terminal coupled to the sixth node, and an output terminal coupled to the sixth node.

16. The circuit of claim 15, wherein the third control signal represents a result of a logical NAND operation between a complement of the first control signal and a complement of the second control signal.

17. The circuit of claim 15, wherein the loop filter comprises:

a first loop filter resistor coupled to the fifth node;

a first loop filter capacitor coupled between the first loop filter resistor and ground; and

a second loop filter capacitor coupled between the fifth node and ground.

18. The circuit of claim 17, wherein the loop filter further comprises:

a second loop filter resistor coupled between the fifth node and a seventh node;

a third loop filter capacitor coupled between the seventh node and ground.

19. A phase locked loop, comprising:

a phase frequency detector (PFD) configured to compare phases of an input signal and a feedback signal, and to generate therefrom control signals;

a logic circuit configured to compare phases of the input signal and the feedback signal, and to generate therefrom a selection signal indicating locking of the phased locked loop;

a charge pump circuit to be selectively coupled in series with the PFD based upon the selection signal indicating that the phase locked loop has not locked and comprising:

first and second current sources;

a loop filter coupled between a voltage controlled oscillator (VCO) control node and a ground node;

a buffer having an input coupled to the VCO control node;

a first switch configured to couple the first current source to the VCO control node such that the voltage at the VCO control node increases, based upon the control signals indicating that the phase of the input signal leads the phase of the feedback signal,

a second switch configured to couple the second current source to the VCO control node such that the voltage at the VCO control node decreases, based upon the control signals indicating that the phase of the feedback signal leads the phase of the input signal;

an attenuation circuit to be selectively coupled in series with the PFD based upon the selection signal indicating that the phase locked loop has locked and comprising:

first and second current sources;

a loop filter coupled between a voltage controlled oscillator (VCO) control node and a ground node;

a buffer having an input coupled to the VCO control node;

an impedance network coupled to the VCO control node and comprising at least one impedance element configured to be:

coupled to the first current source such that voltage at the VCO control node increases, based upon the control signals indicating that the phase of the input signal leads the phase of the feedback signal, and

coupled to the second current source such that the voltage at the VCO control node decreases, based upon the control signals indicating that the phase of the feedback signal leads the phase of the input signal;

a VCO coupled to the VCO control node and to generate an output signal based upon a signal at the VCO control node, the phase of the output signal matching the phase of the input signal;

wherein the feedback signal is based upon the output signal.

20. The phase locked loop of claim **19**, wherein the control signals comprise first and second control signals; wherein the first control signal is asserted based upon the phase of the input signal leading the phase of the feedback signal; wherein the second control signal is asserted based upon the phase of the feedback signal leading the phase of the input signal; and wherein the impedance network further comprises:

a first impedance network switch coupled between a first impedance network node and the VCO control node, the first impedance network switch being actuated based upon a third control signal;

a second impedance network switch coupled between the first impedance network node and a second impedance network node, the second impedance network switch being actuated based upon a complement of the third control signal; and

a third impedance network switch coupled between the second impedance network node and an output of the buffer, the third impedance network switch being actuated based upon the complement of the third control signal;

wherein the at least one impedance element comprises a first capacitor coupled between the second impedance network node and ground, and a second capacitor coupled between the first impedance network node and a second impedance network node.

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